WHAT IS CLAIMED IS:

1. A method of manufacturing a semiconductor device, comprising:

forming a first pattern in a first region over a semiconductor substrate;

forming a second pattern in a second region separated from the first region over the semiconductor substrate;

depositing an interlayer insulation film to cover the first and second patterns;

forming a photoresist film on the interlayer insulation film;

treating the photoresist film in stepper exposure and development to form a photoresist pattern of a photomask having its device pattern matched with the first pattern and its alignment marks matched with the second pattern;

selectively etching off the interlayer insulation film over the first and second patterns, with the photoresist pattern; and

after removing the photoresist pattern, flattening the interlayer insulation film to expose the surfaces of the first and second patterns, respectively.

2. A method according to claim 1, wherein the flattening the interlayer insulation film is performed by chemical mechanical polishing the interlayer insulation film.

3. A method according to claim 1, wherein the photomask is provided with marks for forming inspection targets for misalignment, and the step of forming a second pattern includes, prior to the depositing an interlayer insulation film, forming the second pattern

that matches with the marks for forming inspection targets for misalignment.

4. A method according to claim 1, further comprising: after flattening the interlayer insulation film, removing the first pattern to form trenches, and filling the trenches with a material to create a third pattern.

5. A method according to claim 4, wherein the forming a third embedded pattern includes defining transistor gate electrodes in that pattern.

6. A method according to claim 5, further comprising:
prior to depositing an interlayer insulation film, implanting impurities in the semiconductor substrate to form transistor source and drain regions, with a mask of the first pattern.

7. A method according to claim 4, wherein the removing the first pattern includes simultaneously removing the second pattern to form trenches, and thereafter filling the trenches with the identical material to that for the third pattern.

8. A method according to claim 1, wherein the first and second patterns are simultaneously formed in a single forming using the same material.

9. A method according to claim 1, wherein the photoresist pattern over the second pattern is shaped in an almost cross-like plane pattern.

10. A method of manufacturing a semiconductor device, comprising:

forming dummy gate electrodes in a device formation area of a semiconductor device, and forming a dishing inhibiting pattern in a target area of the semiconductor device;

forming an interlayer insulation film to cover the dummy gate electrodes and the dishing inhibiting pattern;

after covering the interlayer insulation film with a photoresist film, treating the photoresist film in stepper exposure and development to form a photoresist pattern of a photomask having its device pattern matched with the dummy gate electrodes and its alignment marks matched with the dishing inhibiting pattern or having its marks for forming inspection targets for misalignment matched with the same;

selectively etching the interlayer insulation film over the dummy gate electrodes and the dishing inhibiting pattern, with the photoresist pattern;

after removing the photoresist pattern, flattening the interlayer insulation film by means of chemical mechanical polishing to expose the surfaces of the dummy gate electrodes and the dishing inhibiting pattern, respectively; and

removing the dummy gate electrodes and filling with a material to form gate electrodes.

11. A method of manufacturing a semiconductor device, comprising:

forming dummy gate electrodes in a device formation area of a semiconductor device, and forming a dishing inhibiting pattern in a target area of the semiconductor device;

forming a nitride film to cover the dummy gate electrodes and the dishing inhibiting pattern, thereby setting side walls of the nitride film on opposite sides of each of the dummy gate electrodes;

covering the entire surface of the semiconductor substrate with an interlayer insulation film;

after covering the interlayer insulation film with a photoresist film, treating the photoresist film in stepper exposure and development to form a photoresist pattern of a photomask having its device pattern matched with the dummy gate electrodes and its alignment marks matched with the dishing inhibiting pattern or having its marks for forming inspection targets for misalignment matched with the same;

selectively etching the interlayer insulation film over the dummy gate electrodes and the dishing inhibiting pattern, with the photoresist pattern;

after removing the photoresist pattern, treating the interlayer insulation film and the nitride film in chemical mechanical polishing to expose the surfaces of the dummy gate electrodes and the dishing inhibiting pattern, respectively; and

removing the dummy gate electrodes and filling with a material to form gate electrodes.

12. A method of manufacturing a semiconductor device, comprising:

forming dummy gate electrodes in a device formation area of a semiconductor device, and forming a dishing inhibiting pattern in a target area of the semiconductor device;

selectively etching the dishing inhibiting pattern to form pattern trenches;

depositing an interlayer insulation film to cover the dummy gate electrodes and the dishing inhibiting pattern and filling the pattern trenches with the interlayer insulation film to create targets in the dishing inhibiting pattern for alignment with a photomask;

after covering th interlayer insulation film with a photoresist film, treating the photoresist film in stepper exposure and development to form a photoresist pattern of the photomask having its device pattern matched with the dummy gate electrodes and its alignment marks matched with the targets in the dishing inhibiting pattern or having its marks for forming inspection targets for misalignment matched with the same;

selectively etching the interlayer insulation film over the dummy gate electrodes and the dishing inhibiting pattern, with the photoresist pattern;

after removing the photoresist pattern, flattening the interlayer insulation film by means of chemical mechanical polishing to expose the surfaces of the dummy gate electrodes and the dishing inhibiting pattern, respectively; and

removing the dummy gate electrodes to obtain gate trenches and filling the gate trenches with material of electrode to form gate electrodes.

13. A semiconductor device having a first region provided with semiconductor devices and a second region provided with targets for alignment with a photomask, comprising:

a first pattern formed in the first region,

a second pattern formed in the second region,

an interlayer insulation film surrounding the first and second patterns and having its surface flattened, and

alignment targets around the second pattern within lamination of the semiconductor substrate.

14. A semiconductor device according to claim 13, wherein the first pattern is an interconnection.